Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A semiconductor laser device comprising:

a first semiconductor layer made of a nitride based semiconductor and including an active layer;

a striped second semiconductor layer along a <1$\bar{1}$00> direction or <11$\bar{2}$0> direction made of a nitride based semiconductor and formed on said first semiconductor layer; and

a current blocking layer formed on said first semiconductor layer on both sides of said second semiconductor layer,

said second semiconductor layer including a cladding layer which comprises a lower layer having a first width at its lower end and an upper layer having a second width larger than said first width at its lower end, both of said lower layer and said upper layer having a larger band-gap than that of said active layer.

Claim 2 (Original): The semiconductor laser device according to claim 1, wherein

said cladding layer has the function of confining light in said active layer.

Claim 3 (Original): The semiconductor laser device according to claim 1, further comprising

a third semiconductor layer formed on said cladding layer and having a carrier concentration which is not less than that of said cladding layer.

Claim 4 (Original): The semiconductor laser device according to claim 3, wherein said third semiconductor layer is a contact layer.

Claim 5 (Original): The semiconductor laser device according to claim 1, further comprising

a third semiconductor layer formed on said cladding layer and having a smaller band-gap than that of said cladding layer.

B' cont'd

Claim 6 (Original): The semiconductor laser device according to claim 5, wherein said third semiconductor layer is a contact layer.

Claim 7 (Original): The semiconductor laser device according to claim 1, wherein

said lower layer in said cladding layer has said first width which is approximately constant from its lower end to its upper end, and

said upper layer in said cladding layer has a second width which is approximately constant from its lower end to its upper end.

Claim 8 (Original): The semiconductor laser device according to claim 1, wherein

said lower layer in said cladding layer has said first width which is approximately ~~constant from its lower end to its upper end, and~~

said upper layer in said cladding layer has a width which gradually decreases upward from said second width.

Claim 9 (Original): The semiconductor laser device according to claim 1, wherein

said first semiconductor layer comprises a cladding layer of a first conductivity type, said active layer, and a first cladding layer of a second conductivity type in this order from its bottom, and

said second semiconductor layer comprises a second cladding layer of a second conductivity type as said cladding layer.

Claim 10 (Original): The semiconductor laser device according to claim 1, wherein

said first semiconductor layer is a first nitride based semiconductor layer containing at least one of boron, thallium, gallium, aluminum, and indium,

said second semiconductor layer is a second nitride based semiconductor layer containing at least one of boron, thallium, gallium, aluminum, and indium, and

said current blocking layer is a third nitride based semiconductor layer containing at least one of boron, thallium, gallium, aluminum, and indium.

Claim 11 (Currently Amended): A method of fabricating a semiconductor laser device, comprising the steps of:

forming a first semiconductor layer made of a nitride based semiconductor and including an active layer; and

forming a striped second semiconductor layer along a <1$\bar{1}$00> direction or <11$\bar{2}$0> direction made of a nitride based semiconductor on said first semiconductor layer, and

~~forming a current blocking layer on said first semiconductor layer on both sides of said~~ second semiconductor layer,

the step of forming said second semiconductor layer comprising the step of forming a cladding layer which comprises a lower layer having a first width at its lower end and an upper layer having a second width larger than said first width at its lower end, both of said lower layer and said upper layer having a larger band-gap than that of said active layer.

Claim 12 (Original): The method according to claim 11, wherein

the step of forming said second semiconductor layer and said current blocking layer comprises the steps of

forming a current blocking layer on said first semiconductor layer,

forming on said current blocking layer a first mask pattern having a first striped opening,

etching said current blocking layer inside said first striped opening of said first mask pattern by a first depth, to form a striped recess in said current blocking layer,

removing said first mask pattern, and then forming a second mask pattern having a second striped opening wider than said striped recess of said current blocking layer on said current blocking layer on both sides of said striped recess,

etching said current blocking layer inside said second striped opening of said second mask pattern to a second depth at which said first semiconductor layer is exposed, to form in said current blocking layer a striped opening which stepwise widens from a lower end to an upper end of said current blocking layer, and

removing said second mask pattern, and then forming said second semiconductor layer on said current blocking layer and on said first semiconductor layer inside said striped opening of said current blocking layer.

Claim 13 (Original): The method according to claim 11, wherein

the step of forming said second semiconductor layer and said current blocking layer comprises the steps of

forming a current blocking layer on said first semiconductor layer,

forming on said current blocking layer a first mask pattern having a first striped opening and composed of a first material,

forming a second mask pattern having a second striped opening narrower than said first striped opening of said first mask pattern and composed of a second material different from said first material on said current blocking layer inside the first striped opening and on said first mask pattern,

etching said current blocking layer inside said second striped opening of said second mask pattern by a first depth, to form a striped recess in said current blocking layer,

removing said second mask pattern, and then etching said current blocking layer inside said first striped opening of said first mask pattern to a second depth at which said first semiconductor layer is exposed, to form in said current blocking layer a striped opening which stepwise widens from a lower end to an upper end of said current blocking layer, and

removing said first mask pattern, and then forming said second semiconductor layer on said current blocking layer and on said first semiconductor layer inside said striped opening of the current blocking layer.

~~Claim 14 (Original): The method according to claim 11, wherein the step of~~ forming said second semiconductor layer and said current blocking layer comprises the steps of

forming a first current blocking layer on said first semiconductor layer,

forming on said first current blocking layer a first mask pattern having a first striped opening,

etching said current blocking layer inside said first striped opening of said first mask pattern, to form a striped opening in said first current blocking layer,

removing said first mask pattern, and then forming a second semiconductor layer on said first current blocking layer and on said first semiconductor layer inside said striped opening of said first current blocking layer,

forming a striped second mask pattern in a region on said second semiconductor layer above said striped opening of said first current blocking layer,

etching said second semiconductor layer, except in a region of said second mask pattern to expose said first current blocking layer on both sides of said second mask pattern, to form in said second semiconductor layer a lower layer having said first width which is approximately constant from its lower end to its upper end and an upper layer having a width which gradually decreases upward from said second width, and

selectively forming a second current blocking layer on said first current blocking layer, except in a region on said second mask pattern.

Claim 15 (Original): The method according to claim 11, wherein

the step of forming said second semiconductor layer and said current blocking layer comprises the steps of

~~forming on said first semiconductor layer a first mask pattern having a striped~~ opening,

selectively growing a second semiconductor layer on said first semiconductor layer inside said striped opening and on said first mask pattern in the periphery of said striped opening,

removing said first mask pattern, and then forming a second mask pattern on an upper surface of said second semiconductor layer, and

selectively growing a current blocking layer on said first semiconductor layer on both sides of said second semiconductor layer, except on said second mask pattern.

Claim 16 (Original): The method according to claim 11, further comprising the step of

forming on said cladding layer a third semiconductor layer having a smaller band-gap than that of said cladding layer.

Claim 17 (Original): The method according to claim 11, further comprising the step of

forming on said cladding layer a third semiconductor layer having a carrier concentration which is not less than that of said cladding layer.

Claim 18 (Original): The method according to claim 11, wherein

the step of forming said cladding layer comprises the step of forming a lower layer having said first width which is approximately constant from its lower end to its upper end and an upper layer having said second width which is approximately constant from its lower end to its upper end.

Claim 19 (Original): The method according to claim 11,

wherein the step of forming said cladding layer comprises the step of forming a lower layer having said first width which is approximately constant from its lower end to its upper end and an upper layer having a width which gradually decreases upward from said second width.

Claim 20 (Original): The method according to claim 11, wherein

the step of forming said first semiconductor layer comprises the step of forming a cladding layer of a first conductivity type, said active layer, and a first cladding layer of a second conductivity type in this order from its bottom, and

the step of forming said second semiconductor layer comprises the step of forming a second cladding layer of a second conductivity type as said cladding layer.

Claim 21 (Original): The method according to claim 11, wherein

said first semiconductor layer is a first nitride based semiconductor layer containing at least one of boron, thallium, gallium, aluminum, and indium,

said second semiconductor layer is a second nitride based semiconductor layer containing at least one of boron, thallium, gallium, aluminum, and indium, and

said current blocking layer is a third nitride based semiconductor layer containing at least one of boron, thallium, gallium, aluminum, and indium.